Amendments to the Drawings:

The attached sheet of drawings includes changes to FIG. 7. This sheet, which includes FIGS. 6 and 7, replaces the original sheet including FIGS. 6 and 7. In FIG. 7, a typographical error has been corrected.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes

Remarks

This Response is considered fully responsive to the Office Action mailed January 8, 2007. Claims 1-23 were pending in the application. Claims 1-23 stand rejected. In this Response, no claims have been amended, added, or cancelled. Claims 1-23 are now pending in the application. Reexamination and reconsideration are requested.

Objection to the Drawings

The Office has objected to FIG. 7 because of an informality. Specifically, Figure 7, included in sheet 5 of the drawings, included a typographical error in a label. Replacement sheet 5, correcting the typographical error, is submitted herewith. The element in FIG. 7 formerly labeled "TEM" has been amended to be labeled "TEM." Reconsideration and withdrawal of this objection are respectfully requested.

Rejections Under 35 U.S.C. § 102

Claims 1, 3, and 4 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 7,007,201 to Byrne, et al. ("Byrne"). All rejections are respectfully traversed.

Independent claim 1 recites, *inter alia*, "a serial trace port, wherein the serial trace port provides controller trace data and wherein the controller trace data is provided external to the integrated circuit device using a differential serial channel." Claims 3 and 4 depend, either directly or indirectly, from independent claim 1.

The Office contends that the output 108 of Byrne "is interpreted as a differential serial channel," and Byrne at col. 3, lines 34-36 is cited in support of this contention. Applicant, however, respectfully disagrees. Byrne at col. 3, lines 34-36, merely states "The signal TRACE_PORT may convey information that is generally helpful in understanding the operation of the selected processor 12." This provides no teaching or suggestion that output 108 of Byrne is intended to be a differential serial channel. In Byrne, the discussion of output 108 is limited to the statements "The apparatus 100 may have an output 108 to present a signal (e.g., TRACE_PORT)," Byrne at col. 2, lines 55-56, and "The signal TRACE_PORT may be presented by the ETM at the output 108," Byrne at col. 3, lines 33-34. Applicant respectfully submits that, absent some teaching in Byrne, output 108 can not be interpreted as a differential serial channel. Thus, Byrne does not teach all of the limitations of independent claim 1. Accordingly, independent claim 1 and those claims depending directly or indirectly therefrom

are believed to patentably distinguish over the cited art. Reconsideration and allowance of claim 1, and those claims depending therefrom, are respectfully requested.

Regarding claim 3 which recites, *inter alia*, that "the serial trace port also provides controller trace data of the second controller," the Office asserts that Byrne also teaches this feature. Applicant, however, respectfully disagrees. Byrne teaches that "The trace circuit may be configured to present information at a port for debugging software in **a selected processor of the processors**." (Emphasis added.) Byrne, Abstract. According to claim 3, in contrast, the serial trace port provides controller trace data of a first controller **and** controller trace data of a second controller. For at least this reason, and those set forth above, claim 3 and those claims depending directly or indirectly therefrom are believed to patentably distinguish over the cited art. Reconsideration and allowance of claim 3, and those claims depending therefrom, are respectfully requested.

Claim 4 recites, *inter alia*, that "the serial trace port receives a reference clock signal and provides a clock signal to each of the controller and second controller." The Office asserts that Byrne also teaches this feature, citing FIG. 2, reference numeral 104, and col. 3, lines 4-5 of Byrne, and states that "it is interpreted that the entire interface containing all inputs and outputs 104, 106, 108 is considered a serial trace port." Applicant respectfully disagrees and notes that this interpretation of a serial trace port is inconsistent with that asserted by the Office in claim 1, where ETM 14 was interpreted as a serial trace port, and output 108 was interpreted as a differential serial channel.

Byrne at col. 3, lines 4-5 states "The signal TCK received at the interface 104 may be provided to each processor 12A-B and the ETM 14." Signal TCK is a test clock signal. Referring to FIG. 2, cited by the Office, signal TCK is received at the interface 104, and the test clock signal is provided to processor 12A, processor 12B, and ETM 14 directly from interface 104. Byrne provides no teaching or suggestion that a reference clock signal is provided to the serial trace port, and that the serial trace port provides the clock signal to the two controllers. For at least this reason, and those set forth above, claim 4 is believed to patentably distinguish over the cited art. Reconsideration and allowance of claim 4 is respectfully requested.

Rejections Under 35 U.S.C. § 103

Claims 2, 5, 6, 8-11, 13-17, and 19-23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Byrne in view of NS (*SCAN921023 and SCAN921224 20-66 Mhz 10 Bit Bus LVDS*). All rejections are respectfully traversed.

Applicant respectfully submits that NS fails to cure the aforementioned deficiencies of Byrne discussed above. Thus, neither Byrne nor NS teaches or suggest all of the features of dependent claims 2, 5, and 6. Accordingly, Applicants respectfully submit that claims 2, 5, and 6 patentably distinguish over the cited art for at least the aforementioned reasons. Reconsideration and allowance of claims 2, 5, and 6 are respectfully requested.

Further, Applicant respectfully submits that neither Byrne nor NS expressly or impliedly suggest the asserted combinations, as recited in claims 2, 5, 6, 8-11, 13-17, and 19-23. Indeed, Applicant notes no such contention in the Office Action. Thus, as part of its initial burden to establish a *prima facie* case of obviousness, the Office "must present a convincing line of reasoning as to why the artisan would have found the claimed invention to be obvious in light of the teachings of the references." MPEP §2142, citing *Ex Parte Clapp*, 227, USPQ 972, 973 (Bd. Pat. App. & Inter. 1985).

Section 2142 of the Manual of Patent Examining Procedure ("MPEP") explains that a *prima facie* case of obviousness requires that there be some suggestion or motivation, either in the references themselves or in the knowledge of one of ordinary skill in the art, to modify or combine reference teachings. It is for this reason that the mere fact that a combination **can** be made is legally insufficient to support an obviousness rejection. MPEP §2143.01. The Office bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the Office does not produce a *prima facie* case, the Applicant is under no obligation to submit evidence of nonobviousness. MPEP §2142. Applicant respectfully submits that such is the case in the present application.

The Office Action provides a line of reasoning for the alleged motivation to make the asserted combinations. Specifically, the Office repeatedly asserts that the asserted combinations "would have been obvious because the use of a differential transmitter as taught by NS increases the speed at which serial data is transmitted from a testing device to an analyzer, therefore allowing for quicker determination as to whether a device under test is encountering any problems." However, Byrne at col. 1, lines 5-8, specifically states that "The present invention

relates to a method and/or architecture for debugging software in embedded processors generally and, more particularly, to a method and/or architecture for **real time debug** via an external trace port." Thus, it is asserted that one of ordinary skill in the art would have been motivated to modify Byrne's teaching of a method and/or architecture for real time debug in view of NS's teachings to allow for quicker determination as to whether a device under test is encountering any problems.

This line of reasoning, however, does not meet the MPEP's required standard of "convincing" because Byrne provides for real time debug **without the asserted modification**. Stated another way, Byrne alone provides for real time debug and does not teach or suggest the transmission of data from a testing device to an analyzer, no motivation exists to "increase the speed at which data is transmitted from a testing device to an analyzer to allow for quicker determination as to whether a device under test is encountering any problems." Consequently, the Office Action fails to provide the required "convincing line of reasoning" required by the MPEP. The absence of this convincing line of reasoning and any other suggestion for the asserted combinations precludes a *prima facie* case of obviousness.

Further, Applicant submits that the motivation articulated by the Office is based on impermissible hindsight. *See* MPEP §2143.01. An obviousness determination may "take[s] into account only knowledge which was within the level of ordinary skill in the art at the time the claimed invention was made and does not include knowledge gleaned only from applicant's disclosure." *In re McLaughlin*, 443 F.2d 1392, 1395, 170 USPQ 209, 212 (CCPA 1971). In the instant case, the motivation proposed by the Office for combining Byrne with NS appears to be **gleaned directly from Applicant's Specification** and, thus, is impermissible. Specifically, paragraph [0007] of the present pending application states "It would thus be desirable to provide a system and method for providing a debugging environment that uses a high speed serial interface to provide a debug interface between an IC device being debugged and a control console/workstation such that the IC device can run at its normal, high speed, thereby enabling real time emulation of an SOC device having a serial debug port." As the cited references fail to discuss any debug interface between an IC device being debugged and a control console/workstation, no motivation exists to "increase the speed at which data is transmitted from a testing device to an analyzer."

For at least these reasons, and those set forth above, the rejections of claims 2, 5, 6, 8-11, 13-17, and 19-23 under 35 U.S.C. §103 are respectfully traversed. Reconsideration and allowance of the claims are respectfully requested.

Claims 7, 12, and 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Byrne in view of NS, and further in view of U.S. Publication No. 2006/0288254 by Agarwala, et al., ("Agarwala"). All rejections are respectfully traversed.

Applicant respectfully submits that Agarwala fails to cure the deficiencies of Byrne and NS discussed above. Thus, Claim 7 is believed to patentably distinguish over the cited art for at least the same reasons as those claims from which it depends. Reconsideration and withdrawal of the rejection of claim 7 is respectfully requested.

Further, Applicant respectfully submits that there is no "convincing line of reasoning" presented as to the Office's rationale for combining the teachings of Agarwala with Byrne and/or NS, and that the motivation provided by the Office is a product of impermissible hindsight for at least the same reasons as discussed with respect to Byrne and NS. Additionally, the product of Byrne and NS provides for "faster transmission of data" without the modifications taught by Agarwala. Regarding the Office's assertion that combining Agarwala with Byrne and NS would have been obvious because it allows for "conservation of inter/extra-circuit communication bandwidth," Applicant respectfully submits that this alleged motivation is also the product of impermissible hindsight. In the instant case, the motivation proposed by the Office for combining Agarwala with Byrne and NS also appears to be **gleaned directly from Applicant's Specification**. Specifically, the present pending application at paragraph [0031] states "In an alternate embodiment to the present invention, a lossless compression technique such as Huffman or LZW coding is provided to further reduce data transmission bandwidth requirements by reducing the overall amount of data required to be transmitted to the debugging tool 106 (shown in FIG. 1)." As the cited references fail to discuss any debug interface between an IC device being debugged and a control console/workstation or transmission of trace data, no motivation exists to conserve "inter/extra-circuit communication bandwidth."

For at least these reasons, Applicant respectfully submits that the Office has failed to establish a *prima facie* case of obviousness, and claims 7, 12, and 18 patentably distinguish over the cited art. Reconsideration and allowance of claims 7, 12, and 18 are respectfully requested.

Conclusion

Claims 1-23 are currently pending in the application. Applicant has fully responded to each and every objection and rejection in the Office action dated January 8, 2007 and believes that claims 1-23 are in a condition for allowance. Applicant therefore requests that a timely Notice of Allowance be issued in this case.

The Applicant believes no other fees or petitions are due with this filing. However, should any such fees or petitions be required, please consider this a request therefor and authorization to charge Deposit Account No. 50-3199 as necessary.

If the Examiner should require any additional information or amendment, please contact the undersigned attorney. If the Examiner believes any issues could be resolved via a telephone interview, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

Date: 9 April 2007

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